CIRCUIT FOR AND METHOD OF REALIGNING DATA

ABSTRACT

A circuit enabling the realignment of data is described. The circuit generally comprises an input multiplexer receiving a first plurality of input data bytes and a second plurality of input data bytes; a switching controller coupled to the input multiplexer and controlling the output of the data bytes from the input multiplexer; a delay register coupled to the input multiplexer and receiving predetermined bytes of the first plurality of input data bytes; and an output multiplexer coupled to the input multiplexer and the delay register. The output multiplexer receives the predetermined bytes of the first plurality of input data bytes and predetermined bytes of the second plurality of input data bytes.